

What is claimed is:

1 1. An information processor including a central processing unit having an
2 instruction execution module, said central processing unit having a normal mode for
3 operating said instruction execution module and an execution halt mode for halting
4 said instruction execution module; said information processor comprising:

5 a voltage controlling module for causing said instruction execution module
6 to execute a voltage reduction instruction for placing said central processing unit
7 into a low-voltage operation mode in which the operating voltage of said central
8 processing unit is lowered from the operating voltage in said normal mode when
9 said central processing unit switches from said normal mode to said execution halt
10 mode; and

11 a mode controlling module for placing said central processing unit into a
12 low-voltage halt mode in which said instruction execution module is halted under the
13 operating voltage for said low-voltage operation mode when said voltage controlling
14 module places said central processing unit into said low-voltage operation mode.

1 2. The information processor according to Claim 1, wherein: after said voltage
2 controlling module causes said instruction execution module to execute said voltage
3 reduction instruction, said voltage controlling module causes said instruction
4 execution module to execute a halt grant instruction for sending a halt grant signal
5 to said mode controlling module, said halt grant signal allowing said instruction
6 execution module to halt; and said mode controlling module places said central
7 processing unit into said low-voltage halt mode when said mode controlling module
8 receives said halt grant signal.

1 3. The information processing module according to Claim 1, wherein: when said
2 central processing unit receives an interrupt request for resuming said instruction
3 execution module in said low-voltage halt mode, said mode controlling module
4 places said central processing unit into said low-voltage operation mode; and when

5 said mode controlling module places said central processing unit into said
6 low-voltage operation mode in response to said interrupt request, said voltage
7 controlling module causes said instruction execution module to execute a voltage
8 raise instruction for changing the operating voltage of said central processing unit
9 to the operating voltage in said normal mode and places said central processing unit
10 into said normal mode.

1 4. The information processor according to Claim 3, wherein said interrupt
2 request is an interval timer interrupt provided periodically to said central processing
3 unit to cause said instruction execution module to execute periodically a set of
4 instructions for detecting an executable process; and when said mode controlling
5 module places said central processing unit into said low-voltage operation mode in
6 response to said interval timer interrupt, said voltage controlling module causes said
7 instruction execution module to execute said voltage raise instruction to place said
8 central processing unit into said normal mode, provided that an executable process
9 is detected; and if no executable process is detected, said mode controlling module
10 places said central processing unit into said low-voltage halt mode.

1 5. The information processor according to Claim 4, wherein after said
2 instruction execution module completes the process detected in response to said
3 interval timer interrupt, said voltage controlling module causes said instruction
4 execution module to execute said voltage reduction instruction if the time between
5 the completion of said detected process and reception of the next interval timer
6 interrupt exceeds a predetermined value or retains the operating voltage of said
7 central processing unit without causing said instruction execution module to execute
8 said voltage reduction instruction if the time between the completion of said
9 detected process and reception of the next interval timer interrupt does not exceed
10 the predetermined value.

1 6. The information processor according to Claim 1, wherein said central

2 processing unit further has a voltage reduction mode in which said instruction
3 execution module is halt at a low operating voltage compared with the operating
4 voltages in said low-voltage operation mode and said low-voltage halt mode; and
5 when said central processing unit is shifted from said normal mode to said voltage
6 reduction mode, said voltage controlling module retains the operating voltage in said
7 normal mode without causing said instruction execution module to execute said
8 voltage reduction instruction; and said mode controlling module causes said central
9 processing unit to shift from said normal mode to said voltage reduction mode.

1 7. The information processor according to Claim 1, wherein when said voltage
2 controlling module causes said central processing unit to shift from said normal
3 mode to said low-voltage operation mode, said voltage controlling module operates
4 said central processing unit and places said central processing unit into an
5 intermediate-voltage operation mode in which the operating voltage is lower than
6 the operating voltage in said normal mode and higher than the operating voltage in
7 said low-voltage operation mode and then places said central processing unit into
8 said low-voltage operation mode.

1 8. An information processor including a central processing unit having an
2 instruction execution module, said central processing unit having a normal mode for
3 operating said instruction execution module and an execution halt mode for halting
4 said instruction execution module; said information processor comprising:

5 a frequency controlling module for causing said instruction execution module
6 to execute a frequency reduction instruction for placing said central processing unit
7 into a low-frequency operation mode in which the operating frequency of said
8 central processing unit is lowered from the operating frequency in said normal mode
9 when said central processing unit switches from said normal mode to said execution
10 halt mode; and

11 a mode controlling module for placing said central processing unit into a
12 low-frequency halt mode in which said instruction execution module is halted under

13 the operating frequency for said low-frequency operation mode when said frequency
14 controlling module places said central processing unit into said low-frequency
15 operation mode.

1 9. A program for controlling an information processor including a central
2 processing unit having an instruction execution module, said central processing unit
3 having a normal mode for operating said instruction execution module and an
4 execution halt mode for halting said instruction execution module; said program
5 causing said information processor to function as:

6 a voltage controlling module for causing said instruction execution module
7 to execute a voltage reduction instruction for placing said central processing unit
8 into a low-voltage operation mode in which the operating voltage of said central
9 processing unit is lowered from the operating voltage in said normal mode when
10 said central processing unit switches from said normal mode to said execution halt
11 mode; and

12 a mode controlling module for placing said central processing unit into a
13 low-voltage halt mode in which said instruction execution module is halted under the
14 operating voltage for said low-voltage operation mode when said voltage controlling
15 module places said central processing unit into said low-voltage operation mode.

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1 10. A program for controlling an information processor including a central
2 processing unit having an instruction execution module, said central processing unit
3 having a normal mode for operating said instruction execution module and an
4 execution halt mode for halting said instruction execution module; said program
5 causing said information processor to function as:

6 a frequency controlling module for causing said instruction execution module
7 to execute a frequency reduction instruction for placing said central processing unit
8 into a low-frequency operation mode in which the operating frequency of said
9 central processing unit is lowered from the operating frequency in said normal mode

10 when said central processing unit switches from said normal mode to said execution
11 halt mode; and

12 a mode controlling module for placing said central processing unit into a
13 low-frequency halt mode in which said instruction execution module is halted under
14 the operating frequency for said low-frequency operation mode when said frequency
15 controlling module places said central processing unit into said low-frequency
16 operation mode.

1 11. A storage medium on which the program according to one of Claim 9 or 10
2 is stored.

1 12. A control method for controlling an information processor including a central
2 processing unit having an instruction execution module, said central processing unit
3 having a normal mode for operating said instruction execution module and an
4 execution halt mode for halting said instruction execution module; said method
5 comprising:

6 causing said instruction execution module to execute a voltage reduction
7 instruction for placing said central processing unit into a low-voltage operation mode
8 in which the operating voltage of said central processing unit is lowered from the
9 operating voltage in said normal mode when said central processing unit switches
10 from said normal mode to said execution halt mode; and

11 placing said central processing unit into a low-voltage halt mode in which said
12 instruction execution module is halted under the operating voltage for said
13 low-voltage operation mode when said central processing unit is placed into said
14 low-voltage operation mode.

1 13. A control method for controlling an information processor including a central
2 processing unit having an instruction execution module, said central processing unit
3 having a normal mode for operating said instruction execution module and an
4 execution halt mode for halting said instruction execution module; said method

5 comprising:

6 causing said instruction execution module to execute a frequency reduction

7 instruction for placing said central processing unit into a low-frequency operation

8 mode in which the operating frequency of said central processing unit is lowered

9 from the operating frequency in said normal mode when said central processing unit

10 switches from said normal mode to said execution halt mode; and

11 placing said central processing unit into a low-frequency halt mode in which

12 said instruction execution module is halted under the operating frequency for said

13 low-frequency operation mode when said central processing unit is placed into said

14 low-frequency operation mode.